REMARKS

The Office Action dated October 17, 2003, has been received and carefully noted. The amendments made herein and the following remarks are submitted as a full and complete response thereto.

As a preliminary matter, Applicant appreciates the indication of allowable subject matter in claims 31, 32, 36, 37 and 50-53.

Claims 19, 22-23, 25-26, 28-29, 33-34, 38, and 43-49 have been amended. New claims 54-59 have been added. Applicants submit that the new claims as well as the amendments made herein are fully supported in the specification and the drawings as originally filed, and therefore no new matter has been added. Accordingly, claims 19-59 are pending in the present application and are respectfully submitted for consideration.

Claims 23, 26, 29, 34, 48 and 49 were rejected under 35 U.S.C. §112, second paragraph, as being indefinite. In making this rejection, the Examiner took the position that the phrase "a predetermined voltage" lacks proper antecedent basis. Applicant submits that each of claims 23, 26, 29, 34, 48 and 49 has been amended to overcome the formal matter noted in the Office Action. Therefore, it is submitted that the present application is in full compliance with US patent practice, and Applicant respectfully requests that the rejection be withdrawn.

Claims 19-30, 33-36 and 38-49 were rejected under 35 U.S.C. §102(b) as being anticipated by Fischer et al. (U.S. Patent No. 5,889,491). Applicant respectfully submits that each of claims 19-30, 33-36 and 38-49 recites subject matter that is neither disclosed nor suggested by the cited prior art.

Claim 19 recites an input buffer circuit having a differential amplifier circuit, disposed between a first power supply and a second power supply, for receiving first and second input signals and generating an amplified signal corresponding to a voltage difference between the first and second input signals. In addition, the input buffer circuit includes a first circuit, coupled to the differential amplifier circuit, for receiving the amplified signal from the differential amplifier circuit, a second circuit, including an inverter and a MOS transistor, disposed between the first power supply and the second power supply, for receiving the first input signal, and a control circuit for selectively enabling one of the differential amplifier circuit and the second circuit in accordance with a control signal while isolating the other one of the differential amplifier circuit and the second circuit from at least one of the first power supply and the second power supply.

Accordingly, at least one of the essential features of the present invention is a second circuit, including an inverter and a MOS transistor, disposed between the first power supply and the second power supply, for receiving the first input signal. As such, the present invention results in the advantage of having an input buffer circuit with reduced power dissipation.

It is respectfully submitted that the prior art fails to disclose or suggest the elements of the Applicant's invention as set forth in claims 19-30, 33-36 and 38-49, and therefore fails to provide the advantages which are provided by the present application.

Fischer discloses two standard comparators 201, 202 connected to level-sensing circuitry. The first comparator 201 (COMPN) is implemented using n-channel input devices, whereas the second comparator 202 (COMPP) is implemented using p-

channel input devices. The comparator inputs P and N are connected in parallel via lines 209, 210 respectively, with P being an non-inverting input and N being an inverting input. Their outputs, ZN and ZP on nodes 211, 212 respectively, go through a simple multiplexer comprising pass transistors M1, M2, M3 and M4. which of these outputs (ZN or ZP) is selected by the multiplexer to go through to the comparator output node 213 depends on the voltage levels of the Y and YN control signals, which in turn depends on the absolute levels of the inputs (P and N). The absolute level may be considered the magnitude of the input voltage with respect to a power supply voltage, being V_{SS} (ground or zero volts) in the illustrative case.

Applicant respectfully submits that each and every element recited within claims 19, 22, 25, 28, 33, 38 and 43-47 is neither disclosed nor suggested by Fischer. In particular, Applicant submit that the input buffer circuit as recited in the present application is clearly distinct from that which is illustrated by the combination of the cited prior art. Specifically, it is submitted that the cited prior art fails to disclose or suggest at least a second circuit, including an inverter and a MOS transistor, disposed between the first power supply and the second power supply, for receiving the first input signal.

It is submitted that Fischer merely discloses a comparator. Applicant respectfully submits that the comparator of Fischer is neither comparable nor analogous to at least the second circuit of the present invention. In particular, the second circuit of the claimed invention includes an inverter and a MOS transistor. Accordingly, Applicant submits that Fischer fails to disclose or suggest each and every element recited in

claims 19, 22, 25, 28, 33, 38 and 43-47 of the present application, and therefore each of claims 19, 22, 25, 28, 33, 38 and 43-47 is allowable.

As for claims 20, 21, 23, 24, 26, 27, 29, 30, 34-36, 39-42 and 48-49, it is submitted that each of claims 20, 21, 23, 24, 26, 27, 29, 30, 34-36, 39-42 and 48-49 is dependent on independent claims 19, 22, 25, 28, 33 and 38, respectively. As such, each of claims 20, 21, 23, 24, 26, 27, 29, 30, 34-36, 39-42 and 48-49 is allowable due to its dependency on allowable claims 19, 22, 25, 28, 33 and 38, respectively.

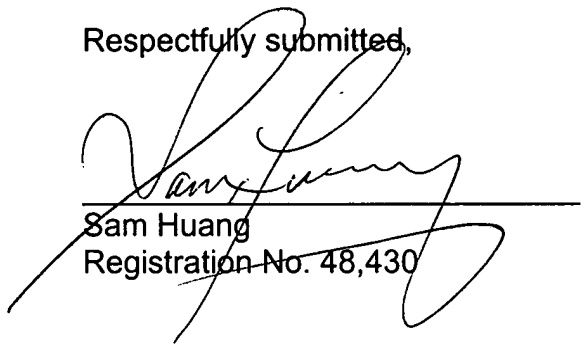
As for new claims 54-59, Applicant respectfully submits that each of new claims 54-59 is dependent on independent claims 19 and 38, respectively. Therefore, each of new claims 54-59 is also allowable due to its dependency on allowable claims 19 and 38, respectively.

In view of the above, Applicant respectfully submits that each of claims 19-59 recites subject matter that is neither disclosed nor suggested in the cited prior art. Applicant also submits that the subject matter is more than sufficient to render the claims non-obvious to a person of ordinary skill in the art, and therefore respectfully request that claims 19-59 be found allowable and that this application be passed to issue.

If for any reason, the Examiner determines that the application is not now in condition for allowance, it is respectfully requested that the Examiner contact the Applicants' undersigned attorney at the indicated telephone number to arrange for an interview to expedite the disposition of this application.

In the event this paper has not been timely filed, the Applicant respectfully petitions for an appropriate extension of time. Any fees for such an extension, together with any additional fees that may be due with respect to this paper, may be charged to counsel's Deposit Account No. 01-2300 referencing Docket Attorney No. 108075-00056.

Respectfully submitted,



Sam Huang
Registration No. 48,430

Customer No. 004372
ARENT FOX KINTNER PLOTKIN & KAHN, PLLC
1050 Connecticut Avenue, N.W., Suite 400
Washington, D.C. 20036-5339
Tel: (202) 857-6000
Fax: (202) 638-4810

SH:grs

TECH/220424.1